Michael Geiger

Master of Science: Electrical Engineering and Information Technology
Web: www.mgeiger.eu
Nationality: German

Address, phone & email not available on public CV.
Please, contact me via my contact form under
https://mgeiger.eu/contact/ to request contact data.

Objective

I want to contribute to your research & development team as a reliable Design & Verification Engineer.

Attributes

Initiative, creative, organized, team worker, strong communicator, attentive to detail, problem solver

Consulting Experience

Self Employed Senior Engineering Consultant *PT-Oporto*

Offering engineering consulting services based on my professional background. Consulting international clients on digital design for ASIC or FPGA, design verification including UVM tests, and flow automation.

zGlue Inc.
Senior Engineering Consultant for Flow Automation and Design Verification *Since May 2019*

Created and implemented concept for fully automated mixed-signal verification flow, based on UVM testbench. Enabled said flow to be called by web-interface, respecting user interaction requirements. Extended and improved test coverage. Optimized performance and resource usage of whole flow. Providing ongoing maintenance and extension support for said flow. Operated self-responsibly, under weekly reporting.

Employment Experience

Intel Corporation *DE-Munich*
Digital Design Engineer *Oct 2017 - Feb 2019*

Joined Intel Munich RF solutions, 4G/5G team. Worked on Digital Design for DfT and MBIST modules. Designed test flows for DfT and MBIST to fully prepare testpattern and simulate automatically. Optimized resource usage and simulation speed. Supported production test engineers with speed optimization. Designed digital components for mixed-signal controller in both data path and control path.
Had first exposure to project management. Prepared and drove plan of chip design language translation. Controlled interns and junior engineers working on design translation. Measured and reported project progress.

Intel Corporation *IE-Dublin*
Hardware Engineer (IC-Design) *Nov 2016 - Sep 2017*

Intel acquired Movidius. Moved on from blocklevel to toplevel design verification. Worked on verification of CPU cores, bus infrastructure, network-on-chip and VLIW-DSP. Studied and modified existing testcases to meet new design. Designed new testcases in C to test new architectural features. Debugged throughout all simulation flow. Found and fixed bugs on every level: highlevel-C, compiler, assembler, linker-scripts, baremetal drivers, register maps, makefile settings, wrong cache configurations etc. Additionally had exposure to machine vision software kernel debugging, power-islands-, cache- and multi-CPU tests. Worked on simulations of every level: RTL-, gate- and power-aware-gate-level. Improved Linux simulation environment and build-flow to use up less resources and run faster. Planned concept of new data type in object-oriented multithreaded C-model framework. Designed and tested custom I2C-slave register interface.

Movidius Ltd. *IE-Dublin*
Junior Verification Engineer *Nov 2015 - Nov 2016*
Joined Movidius' computer vision ASIC design team. Worked on VLIW-DSP-architecture. Implemented features in RTL, such as fast clock gating and instruction extensions. Had exposure to every unit and every pipeline stage of DSP. Improved and fixed design when bugs were discovered. Extended and modified cycle accurate C-model. Improved C-model. Designed directed blocklevel testcases in ASM. Extended coverage of CRT testbenches to test design more comprehensively, with less exceptions. With Movidius, I learned about responsibility as an ASIC developer, how to approach problems individually or in a team and how to work on site or remotely.

Institute for Information Processing Technologies (ITIV) *DE-Karlsruhe*
Assistant Research Scientist - InvasIC project - Microarchitecture *2012-2014*
Extended Leon3 pipeline. Implemented new features into CPU-pipeline. Modified compiler accordingly. Tested new features with self-written Assembler programs in ModelSim.

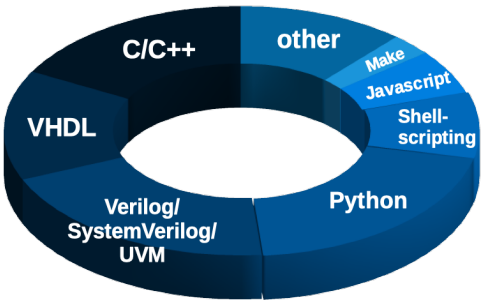
Xilinx Inc. *IE-Dublin*
Research Scientist Intern - Research Labs Department *Feb 2013 - Jul 2013*
Modelled hardware blocks in SystemC and C++. Worked on low level benchmarks in C. Set up a toplevel system of delivered hardware blocks from colleagues. Tested the VHDL and Verilog system in ModelSim. Finally implemented the hardware project on Xilinx Zynq SoC. Presented results in internal conferences.

Institute for Information Processing Technologies (ITIV) *DE-Karlsruhe*
Assistant Research Scientist - Accordance project - RTL Developer *2012-2013*
Designed, implemented and tested an interface for board-to-board communication with high-speed transceivers on FPGAs. Designed customizable low-latency, high-bandwidth, fault-tolerant protocol layer.

Tool Exposure

General	Good knowledge of Linux, Microsoft Office
Cadence Tools	Simvision, Xcelium Simulator
Synopsys Tools	DVE, VCS, Design Compiler, DesignWare IP
Xilinx Tools	Vivado, ISE, Platform Studio, SDK, iSim
Other Tools	Svn, Git, ModelSim, Bugzilla, Clearcase

Language Exposure



Education

Karlsruhe Institute of Technology (KIT) *DE-Karlsruhe*
Master of Science in Electrical Engineering and Information Technology *2012-2015*
Bachelor of Science in Electrical Engineering and Information Technology *2007-2012*
Master profile: *System on Chip*, relevant classes: Numerous classes about Software, Hardware and System Design, Integrated Circuits, Signal Processing, Communication Technology and Computer Science.

Institute for Information Processing Technologies (ITIV) *DE-Karlsruhe*
Master Thesis - InvasIC project - Microarchitecture *2015*
Developed concept to accelearte software loops in hardware. Designed and implemented accelerator.

Institute for Information Processing Technologies (ITIV) *DE-Karlsruhe*
Bachelor thesis - KAHRISMA project - Chip Architecture *2011*
Changed instruction format throughout VLIW-architecture. Developed new exception handling unit.

Language Levels

German	*Native*	**Portuguese**	*Conversationally fluent*
English	*Professional*	**Spanish**	*Conversationally fluent*